AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (*Currently Amended*) A method of transmitting data traffic ~~having a predetermined minimum transmittable element such as any one of a slot and a bit and being~~ received from a plurality ~~number~~ of prioritized ~~prioritised~~ sources, wherein the method comprises ~~comprising the steps of~~:

(a) setting the highest priority source with data traffic waiting for transmission as a current transmission source;

(b) transmitting the data traffic from the current transmission source until completion while ~~whilst~~ monitoring the remaining sources for waiting data traffic, wherein if traffic is detected from a source with a higher priority than the current transmission source, completing transmission of the minimum transmittable element from the current transmission source prior to starting transmission of data traffic from the source with higher priority~~going to step (d)~~;

(c) upon completion of the transmission of data traffic from the current transmission source, going to step (a)~~; and~~,

wherein step (b) comprises adapting control data within the data traffic itself before transmission to comprise, where not already present, at least one reassembly indicator for use in reassembling the data traffic upon receipt~~(d) completing transmission of the current minimum transmittable element and going to step (a)~~.

2. (*Cancelled*).

3. (*Currently Amended*) The ~~A~~ method according to claim 1, in which the minimum transmittable element for data traffic of asynchronous and bit-synchronous protocols is a bit.

4. (*Currently Amended*) The ~~A~~ method according to claim 1, in which the minimum transmittable element for data traffic of slot-synchronous protocols is a slot.

5. (*Currently Amended*) A method of reassembling a number of traffic streams interleaved within a data stream into a respective output queue for each traffic stream, wherein the method comprises ~~comprising the steps of~~:

(a) clearing the output queues and selecting a first output queue for receiving the data stream;

(b) passing the data stream to the selected output queue while ~~whilst~~ monitoring the data stream, and going to step (c) upon detection of a start indicator of a new traffic stream different from the traffic stream currently being received, wherein the start indicator of the new traffic stream is located after the minimum transmittable element of the currently received traffic stream and control data within the new traffic stream itself is adapted to comprise at least one reassembly indicator for use in reassembling the new traffic stream upon receipt, and going to step (d) if the end of a traffic stream is determined;

(c) selecting a further output queue to receive the new traffic ~~data~~ stream and going to step (b); and

(d) if the memory stack contains one or more identifiers of output queues, retrieving the top identifier from the queue, selecting the output queue corresponding to the identifier to receive the traffic ~~data~~ stream and going to step (b), otherwise going to step (a) ~~otherwise~~.

6. (*Currently Amended*) A switch comprising:

a plurality ~~number~~ of memory devices defining queues ~~(1-4)~~ for receiving traffic to be switched, wherein each queue is ~~having an~~ associated with a predetermined priority classification, and

a processor for controlling the transmission of traffic from the queues ~~(1-4)~~ to an output ~~(5,6), the processor being configured to transmit traffic from the higher priority classified queues before traffic from lower priority classified queues, the traffic having a predetermined minimum transmittable element such as any one of a slot and a bit,~~ wherein the processor monitors ~~is configured to monitor~~ the queues ~~(1-4)~~ to determine whether traffic has arrived at a queue having a higher priority classification than the queue from which traffic is currently being transmitted, and if traffic arrives in a queue that has a higher priority than the queue from which traffic is currently being transmitted, the processor suspends ~~being responsive to suspend~~ the current transmission after transmission of the ~~current~~ minimum transmittable element from the lower priority queue and transmits ~~if traffic has arrived at a higher priority classified queue and thereafter transmit~~ traffic from the higher priority ~~that~~ queue, and subsequently resumes ~~resume~~

the suspended transmission after completing transmission of the higher priority traffic, wherein, prior to transmission, the processor adapts control data within the traffic itself to comprise, where not already present, at least one reassembly indicator for use in reassembling the traffic upon receipt.

7. (*Cancelled*).

8. (*Currently Amended*) The ~~A~~ switch according to claim 6[[7]], wherein ~~in which~~ the reassembly indicators comprise different start ~~(7)~~ and end ~~(9)~~ indicators for each cell or packet in the traffic.

9. (*Currently Amended*) The ~~A~~ switch according to claim 6[[7]], wherein ~~in which~~ the reassembly indicators comprise start ~~(7)~~ and length indicators for each cell or packet in the traffic.

10. (*Currently Amended*) The ~~A~~ switch according to claim 6[[7]], wherein ~~in which~~ the reassembly indicators indicate ~~include~~ the queue's priority classification.

11. (*Currently Amended*) The ~~A~~ switch according to claim 9, wherein ~~in which~~ the processor adapts ~~is configured to adapt~~ each packet or cell in the traffic received from the queues to include an indication of the queue's priority classification.

12. (*Currently Amended*) The ~~A~~ switch according to claim 6, wherein the processor stores ~~is configured to store~~ predetermined details of interrupted traffic transmissions and their respective queues in one of the memory devices and retrieves ~~to retrieve~~ the details for use in resuming the interrupted transmission once the interrupting transmission is completed.

13. (*Currently Amended*) The ~~A~~ switch according to claim 6, further comprising a number of outputs, wherein the processor transmits ~~is configured to transmit~~ traffic to an appropriate output depending upon ~~in dependence on~~ the traffic's destination address.

14. (*Currently Amended*) The ~~A~~ switch according to claim 6, wherein ~~in which~~ the minimum transmittable element for traffic of asynchronous and bit-synchronous protocols is a bit.

15. (*Currently Amended*) The ~~A~~ switch according to claim 6, wherein ~~in which~~ the minimum transmittable element for traffic of slot-synchronous protocols is a slot.

16. (*Currently Amended*) A switch comprising an input from which a data stream is received, the data stream comprising interleaved portions of different traffic streams, a number of output queues ~~(30-60)~~ and a processor ~~(20), wherein the processor is~~ configured to separate the interleaved traffic into respective ones of the output queues for reassembly of individual traffic streams from the data stream, wherein the processor monitors the data stream while routing a traffic stream to an output queue until the processor detects a start indicator of a new interleaved portion of traffic stream located after the minimum transmittable element of the currently received data stream and control data of the new traffic stream is adapted to comprise at least one reassembly indicator for use in reassembling the new traffic stream upon receipt, wherein the processor routes the new interleaved portion to another output queue until the end of new interleaved portion is determined, thereafter the processor routes prior data stream to the prior output queue, or until another start indicator of another new interleaved portion of a traffic stream is detected within the data stream, wherein the processor routes the new interleaved portion to a further output queue.

17. (*Cancelled*).

18. (*Currently Amended*) The ~~A~~ switch according to claim 16[[17]], in which the end of an interleaved portion of traffic is determined in dependence on a portion length indicator within the interleaved portion of traffic.

19. (*Currently Amended*) The ~~A~~ switch according to claim 16[[17]], in which the end of an interleaved portion of traffic is determined from end indicator within the data stream.

20. (*Currently Amended*) The ~~A~~ switch according to claim 16[[17]], in which each interleaved portion of traffic comprises ~~includes~~ a priority indicator, wherein the end of an interleaved portion of traffic is determined from a drop in level of the priority indicator.

21. (*Currently Amended*) The ~~A~~ switch according to claim 16[[17]], in which each interleaved portion of traffic comprises ~~includes~~ a priority indicator, wherein a start indicator comprises a rise in the level of the priority indicator.

22. (*Currently Amended*) The ~~A~~ switch according to claim 16[[17]], in which the processor operates ~~(20) is configured to operate~~ as a state machine.

23. (*Currently Amended*) A telecommunications network comprising a switch as claimed in ~~of~~ claim 6.

24. (*Previously Presented*) A computer program product comprising a number of computer executable instructions for executing the steps of claim 1.